16.00hrs 9th OCT 2015 week 2

Jed G. Gibbs
for
Charlton
Rodda

$A \cdot 0 = 0$ $\quad A + 0 = A$

$A \cdot 1 = A$ $\quad A + 1 = 1$

$A \cdot A = A$ $\quad A + A = A$

$A \cdot \bar{A} = 0$ $\quad A + \bar{A} = 1$

Boolean Algebra

Valid for OR, AND, XOR

- Associative

$A + (B + C) = (A + B) + C$

$A \cdot (B \cdot C) = (A \cdot B) \cdot C$

- Distributive

$A \cdot (B + C)$ ... see slide

- Commutative

$A + B = B + A$

DeMorgan's Theorums

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

$\overline{A \cdot}$ (see slide)

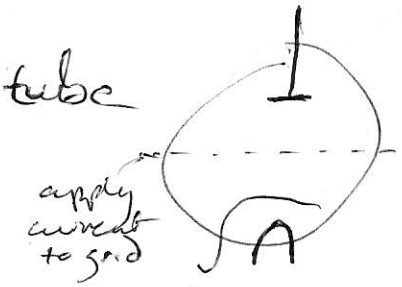
Consequence:

OR can be made with NAND
as a universal gate.

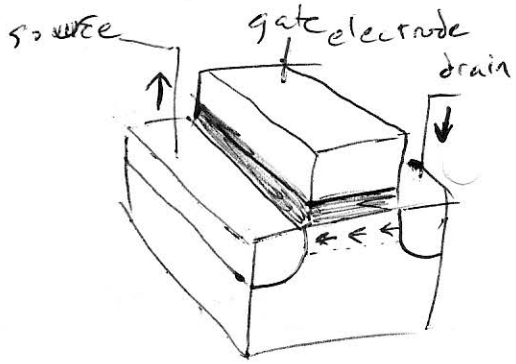
Performing logic in hardware ...

First transistor 1947
using Germanium

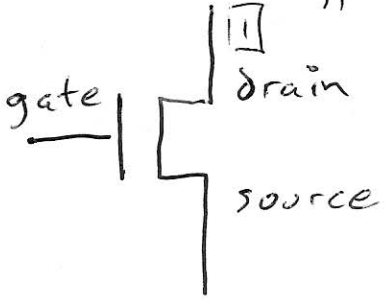
previously valves in glass tube

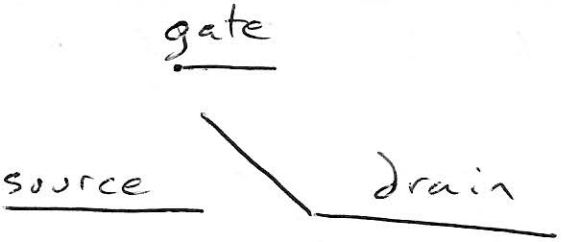


MOS transistor



MOS : Metal-Oxide-Semiconductor
FET : Field-Effect Transistor





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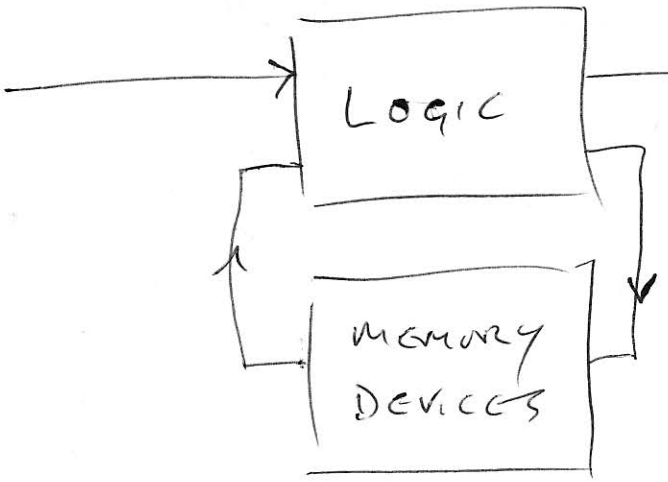
BI-POLAR GERMANIUM is faster than silicon but no use for integrated circuits.

* READING - Stallings chapter 3

Flip flops & Registers

↓ store 1 bit synchronous digital circuits

↓ store the data being worked on in CPUs fastest type of storage

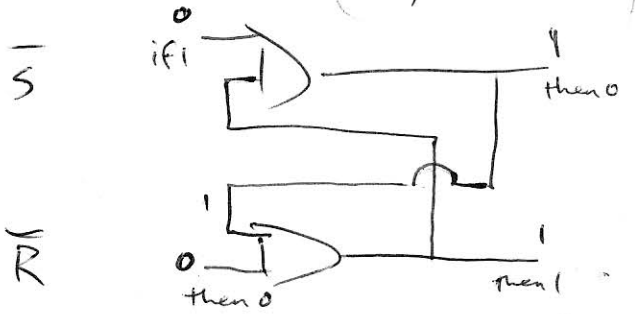


→ output is a function of inputs + stored information

memory accessed at discrete intervals set by 'clock' speed.

Reset-Set flip flop (RS)

(asynchronous)



S	Q
R	Q̄

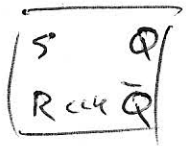
S	R	Q_{N+1}
0	0	Q_N
0	1	0
1	0	1
1	1	undef

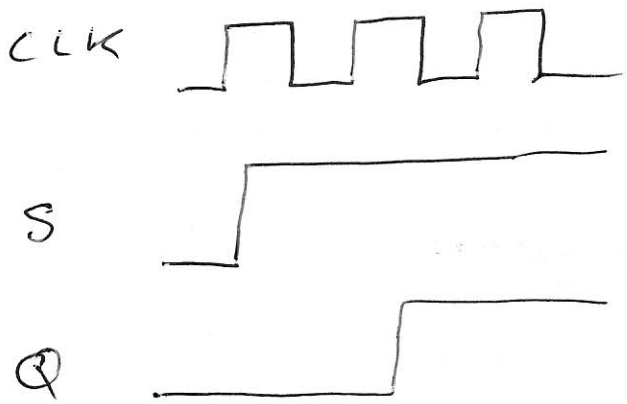
if 1 on both inputs → unpredictable and risk of metastability

THIS HAS TO BE AVOIDED

Clocked RS bistable

- state changes on clock edge





"clock similar to drum on a roman galley
- there to keep the beat + all actions in sync - otherwise you might be trying to read an in-between value"

D-type "Flip Flop"

see slide