16 OCT 2015 10 am

COMPUTER SYSTEMS wk 3

Jed Gibbs for Charlton Rodda

CENTRAL PROCESSING UNITS

CPU's

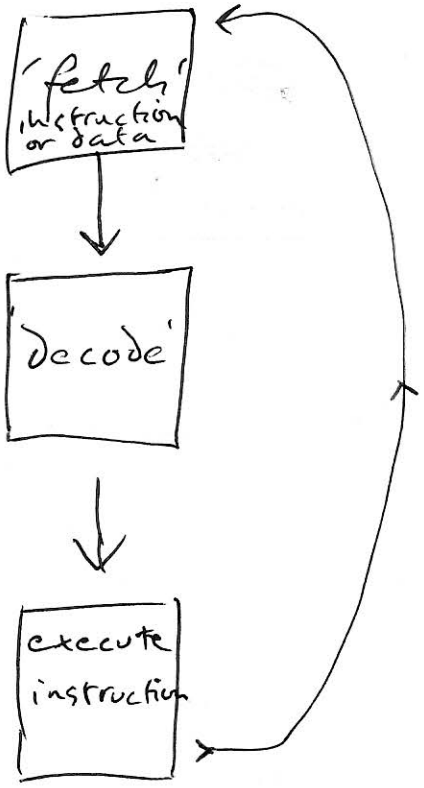
Instructions: simplified example:

Opcode	Mode	register	Address

Although mode varies, the other 3 are sufficiently uniform across CPU's that compilers are able to target the CPU satisfactorily.

CPU goes to a memory address to 'fetch' the instruction from RAM.

[see CPU structure slide from Stalling]



fetch instruction
interpret "
fetch data
process data
write data

Registers

CPU needs temporary storage as working space
called registers → 32/64 bits

this is one of the major design decisions as number + function of registers vary between processor designs.

Top level of the 'memory hierarchy'

User visible registers

General Purpose	Data	Address	Condition Codes
sometimes includes restricted use (booting etc) for data or addressing	(Accumulator in old designs)	(segment or address)	

How many Registers?

Typically 8, 16, 32 or 128 (Titanium)

Too few leads to more memory references

But additional to needs will not reduce memory calls + takes up processor real estate.

(see also RISC)

How Big?

Need to be large enough to hold full address, full word, often possible to combine 2 data registers: int 32 ;
int 16 b
int 64

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Condition Code Registers

sets of individual bits eg result of last operation was zero
(see slide too!)

Control + Status Registers

Program counter

instruction decode register

memory address register

memory buffer register

Program Status Word

You can make use of status words such as if this reaches zero; comparing two values as Equal; continue subtracting until Sign is negative (below zero)