

16 OCT 2015  
16:00hrs wk 3

Kirk Martinez  
COMPUTER  
SYSTEMS

Jed Gibbs

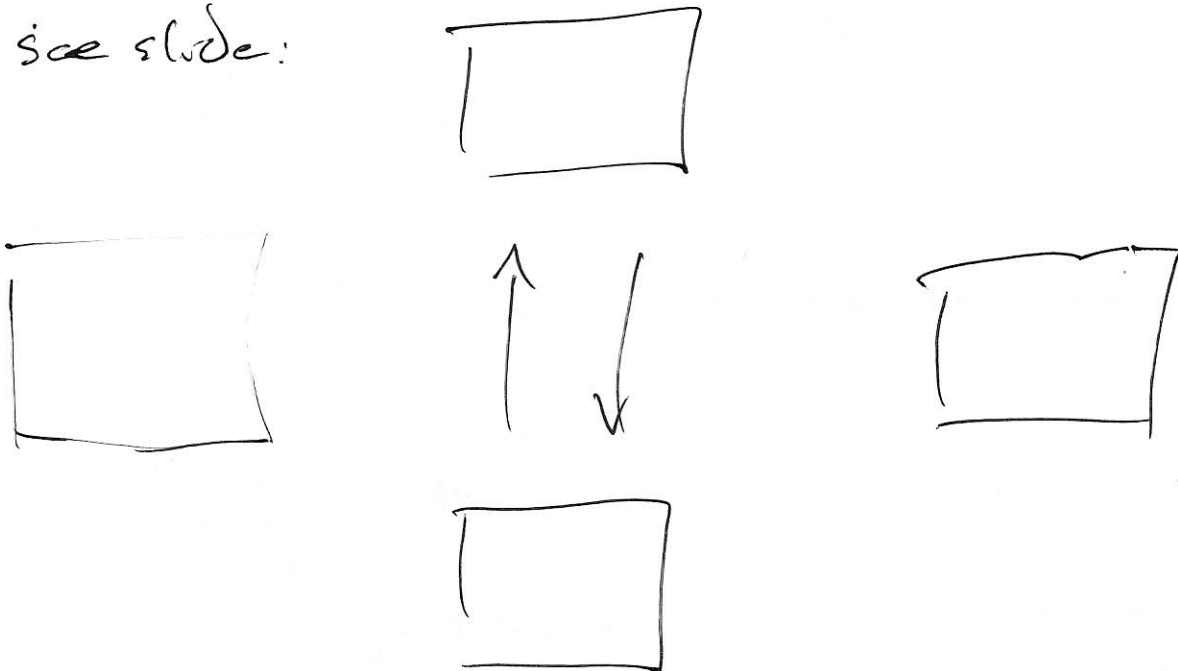
YouTube link to CPU How a CPU works  
link available under CPU instructions

### Indirect Cycle

may require memory access to

Instruction Cycle with Indirect

see slide:



## Instruction Cycle State Diagram

Interrupts about 60 times/second may stop the program for a while, while running a subroutine (transferring info from a disc for example).

At end of instruction cycle the last stage is to increment the PC (Program Counter)

Data Flow. MBR = Memory Buffer Register  
MAR = " Address "  
IR = instruction "  
ALU = Arithmetic Logic Unit

### Prefetch

can fetch next instruction during execution of current instruction.

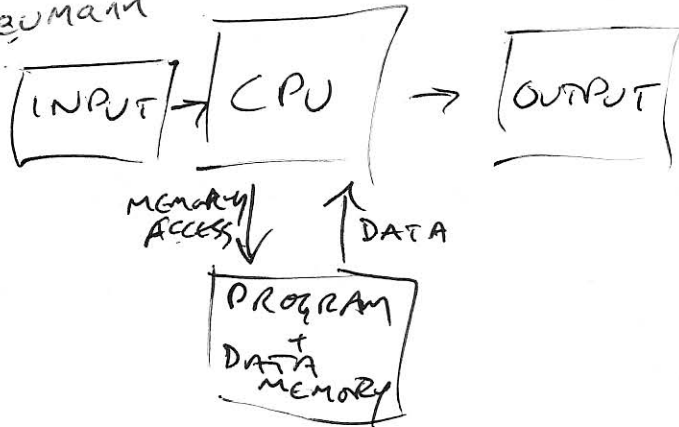
Pentium 3 first mass-market with prefetch?

Prefetch improves performance but not doubled.

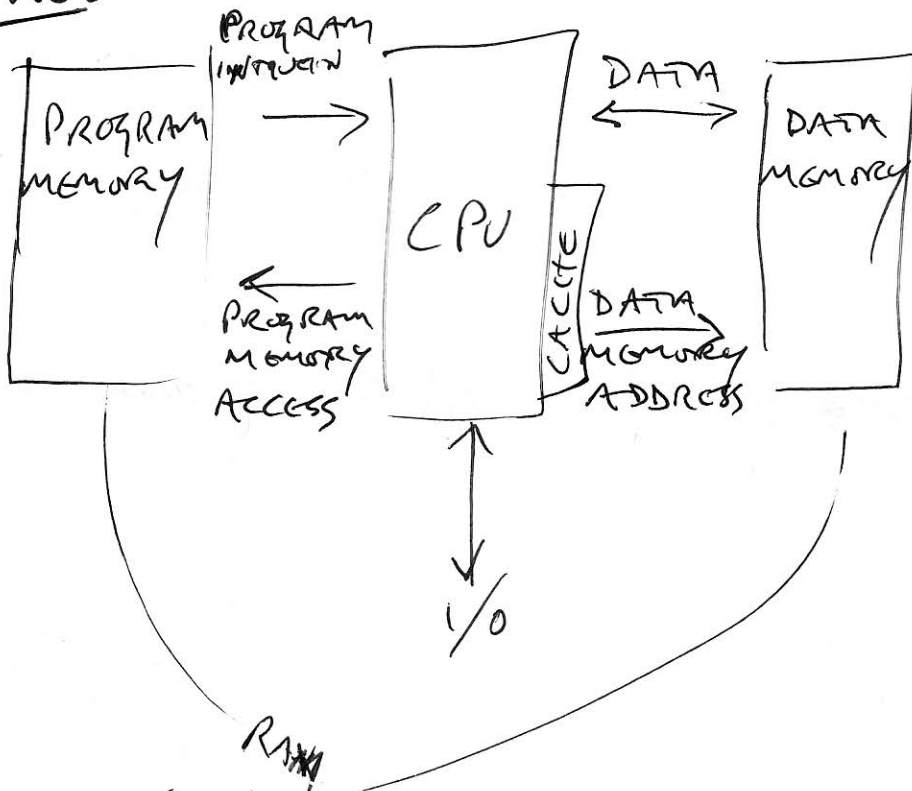
Fetch usually shorter than execution.

# Von Neumann, Harvard, CISC + RISC

## Von Neumann



## Harvard



(see slides)

## CISC + RISC

Berkeley group coined RISC and made cpu RISC1  
soon after Stanford made singular cpu MIPS  
Sun produced SPARC

early RISC cpus had 50 instructions rather than 300  
aimed to simplify CPU to process + sort faster

Aimed to achieve lots of shorter instructions in single clock cycles. via RISC

1. instructions of fixed length
2. Pipelines to achieve the instruction/cycle
3. Simple control logic to increase clock speed. NO microcode
4. operations local

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## CISC

1. Binary compatibility (over 20 years) / RISC (needed recompiling)
2. Complex control logic to control many instructions

Chapter 13 of the book (Stallings)

wikipedia good on RISC