30 Oct 2015 Friday COMP1203 Jed Gibbs

Computer Systems wk5

16:00hrs

examples:

UltraSparc III 6 pipelines: 2 int ALU's
RISC 2 FPU (floating point)
1 load store
1 addressing unit.

MIPS R10000 used in PlayStation 1 + 2
state of the art RISC 64 bit paths
- also in silicon graphics workstations
4 way superscalar, allowed out of order execution
off-chip caches.

POWERPC 604 (used in Apple Macs) RISC

has reservation stations prepping info to put down the pipeline.. Has prefetcher and branch processing unit.

PENTIUM 4 from 2000 AD/ACE
2 x int ALUs, pipeline 20 deep (problem when it stalls!)
dynamic branch predictor etc. (see coloured slide)
Splits FPU from integer processing.

CLOCK RATE only part of the story - DEC Alpha returned better results per clock cycle than P III for example.

(Read Stallings ch13).

Interrupts.

Why? A method for external info from a hard-drive or USB stick etc to interrupt sequence of processing so CPU does not have to wait for slow I/O/Out

can be triggered by program - overflow; division by zero; timers, preemptive multitasks; I/O/out such as mouse; keyboard; network; etc

Interrupt Cycle

- save the context while interrupt runs its own code, then restores previous state.

Multiple Interrupts

Interrupts can themselves be interrupted

- priorities need to be set, such as pressing interrupt button, excessive temperature reading from CPU.

Interrupt Driven I/O

- better than having CPU constantly polling for an interrupt.

http://en.wikipedia.org/wiki/Interrupt